REMARKS

Claims 1 and 2 have been amended, and claims 12 - 15 have been added in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention. It is believed that this Amendment is fully responsive to the Office Action dated June 19, 2002.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

Claims 1 - 6 are currently pending in this patent application, claims 7 - 11 having been withdrawn as non-elected claims in the applicants' Response to Restriction Requirement filed May 31, 2002. Claims 12 - 15 have been added in this Amendment.

As to the merits of this case, claims 1 - 6 stand rejected under 35 USC §103(a) based on Webb (U.S. Patent No. 5,479,031) in view of Planey (U.S. Patent No. 3,772,577). The applicants respectfully request reconsideration of this rejection.

Significant structural arrangements of the applicants' semiconductor device include the PN junction formed, between the first and second base layers 13a, 13b on the inside portion of the first

and second moats 25a, 25b and the first and second buried layers 12a, 12b, as a planar junction.[1]

On the other hand, in the primary reference of Webb, (as can be seen in each of Webb's Figures 1 - 5), upper and lower base regions can be found on respective sides of a mid-region layer, the mid-region layer having buried regions, and the upper base region having emitter regions. For example, in Webb's Figure 2, upper base region 40 is on one side of the mid-region layer 44, while the lower base region 46 is on another side of the mid-region layer 44. The mid-region layer 45 possesses buried regions 42, while the upper base region 40 possesses emitter regions 39. (In each of the embodiments illustrated in Webb's Figures 4 and 5, both the upper and lower base regions contain emitter regions.)

The applicants respectfully submit, however, that the applicants' first and second buried layers 12a, 12b extend, respectively, along first and second base layers 13a, 13b so that, as noted above, the PN junction formed therebetween is "a planar junction."

On the other hand, Webb's buried regions (e.g., buried regions 42, 72, 102, 119, 140, 160) are in discrete forms so as to be "substantially aligned with the shorting dot regions."[2]

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[1] See, e.g., the paragraph bridging pages 18 and 19 of the applicants' specification.

[2] See, lines 10 - 14, column 7 in Webb for, for example, buried regions 42.

Based on the above-discussed teachings of the primary reference of Webb, the applicants have amended independent claim 1 in order to highlight the formation of the "PN planar junctions" between the base layers and the buried layers, and to further highlight in independent claim 1 that the formation of the PN planar junctions is "along the first and second base layers and the first and second buried layers."

As to the secondary reference of Planey, the Examiner specifically relies on this secondary reference for the specific reasons set forth in the paragraph bridging pages 3 and 4 of the outstanding Action. However, such teachings of the secondary reference of Planey do not supplement the above-discussed deficiencies or drawbacks in the teachings of the primary reference of Webb in fully meeting the applicants' claimed semiconductor device, as set forth in amended claim 1 as filed herewith.

As such, even if, *arguendo*, the teachings of Webb and Planey can be combined in the manner suggested by the Examiner, such combined teachings would still fall far short in fully meeting the applicants' claimed invention, as now set forth in amended independent claim 1. Accordingly, a person of ordinary skill in the art would not have found the applicants' claimed invention, as now set forth in amended independent claim 1 and the claims dependent therefrom, obvious under 35 USC §103(a) based on the teachings of Webb and Planey, singly or in combination.

In view of the above, the withdrawal of the outstanding obviousness rejection under 35 USC §103(a) based on Webb (U.S. Patent No. 5,479,031) in view of Planey (U.S. Patent No. 3,772,577) is in order, and is therefore respectfully solicited.

As to the added claims, the applicants respectfully submit that Planey discloses that a moat is, as pointed out by the Examiner, formed, the moat being only formed on one face. Moreover, Planey's moat surrounds P- region 6 (i.e., base region), N+ region being located at the outer periphery of the moat. For such a structural arrangement, it is a necessary photolithographic process to form P-region 6. As a result, a product step is increased for Planey.

As to the applicants' claimed invention, as set forth in added independent claim 12, a first moat is formed on the surface of the first base layer, and a second moat is formed on the surface of the second base layer. Both of the inner periphery and the outer periphery of the first moat are in contact with the first base layer, and both of the inner periphery and the outer periphery of the second moat are in contact with the second base layer. Thus, it is unnecessary to pattern the first and second base layers.

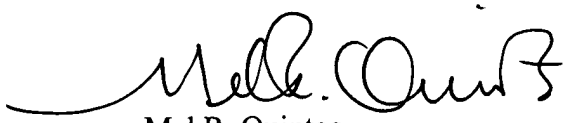
As such, the applicants respectfully submit that the claimed invention, as set forth in added claims 12 - 15, is not disclosed in Webb and Planey, singly or in combination. It is thus respectfully requested that added claims 12 - 15 be similarly allowed.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants' undersigned attorney at the telephone number indicated below to arrange for an interview in order to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicants' respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper to Deposit Account No. 01-2340.

Respectfully Submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



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Enclosures: Version with markings to show changes made

VERSION WITH MARKINGS TO SHOW CHANGES MADE 10/014,407

IN THE CLAIMS:

Please amend claims 1 and 2 as follows:

1. (Amended) A semiconductor device having, when one of either an N-type or P-type is defined as a first conductivity type, and the other is provided as a second conductivity type, a semiconductor substrate of the first conductivity type, the semiconductor device comprising:

first and second buried layers provided within the semiconductor substrate, being of the first conductivity type, and being of a higher concentration than the semiconductor substrate;

first and second emitter layers of the first conductivity type;

first and second base layers of the second conductivity type;

and a substrate layer constituted by the semiconductor substrate,

wherein the substrate layer is sandwiched between the first and second buried layers,

wherein the first and second base layers are positioned on one side surface and the other side surface of the semiconductor substrate so as to form PN planar junctions with the first and second buried layers along the first and second base layers and the first and second buried layers,

wherein the first and second emitter layers are located in a vicinity of a surface of inside of the first and second base layers so as to form PN junctions with the first and second base layers

wherein at least a part of the first and second base layers are respectively provided between the first and second emitter layers and the first and second buried layers, and

wherein at least a part of the first and second buried layers are located between the first and second base layers and the substrate layer.

2. (Amended) The semiconductor device of claim 1, wherein [first and second metal films are formed on both sides] first metal film is formed on the one side of the semiconductor substrate, and second metal film is formed on the other side of the semiconductor substrate, and the first emitter layer and the first base layer being electrically short-circuited by the first metal film, and the second emitter layer and the second base layer being electrically short-circuited by the second metal film.

Please add claims 12 - 15 as follows:

12. A semiconductor device having, when one of either an N-type or P-type is defined as a first conductivity type, and the other is defined as a second conductivity type,

a semiconductor substrate of the first conductivity type, the semiconductor device comprising:

first and second buried layers provided within the semiconductor substrate, being of the first conductivity type, and being of a higher concentration than the semiconductor substrate;

first and second emitter layers of the first conductivity type;

first and second base layers of the second conductivity type;

a substrate layer constituted by the semiconductor substrate,

ring-shaped first moat is provided on the surface of the first base layer,

and ring-shaped second moat is provided on the surface of the second base layer,

wherein the substrate layer is sandwiched between the first and second buried layers,

wherein the first and second base layers are positioned on one side surface and the other side surface of the semiconductor substrate so as to form PN junctions with the first and second buried layers,

wherein the first and second emitter layers are located in a vicinity of a surface of inside of the first and second base layers so as to form PN junctions with the first and second base layers,

wherein at least a part of the first and second base layers are respectively provided between the first and second emitter layers and the first and second buried layers, and

wherein at least a part of the first and second buried layers are located between the first and second base layers and the substrate layer,

wherein the first moat having bottom surfaces reaching the first buried layer, and both outer periphery and inner periphery of the first moat are in contact with the first base layer,

wherein the second moat having bottom surfaces reaching the second buried layer, and both outer periphery and inner periphery of the second moat are in contact with the second base layer.

13. The semiconductor device of claim 12, wherein first metal film is formed on the one side of the semiconductor substrate, and second metal films is formed on the other side of the semiconductor substrate respectively, the first emitter layer and the first base layer being electrically short-circuited by the first metal film, and the second emitter layer and the second base layer being electrically short-circuited by the second metal film.

14. The semiconductor device of claim 12, wherein the first emitter layer is located in a region surrounded by the first moat, and the second emitter layer is located in a region surrounded by the second moat.

15. The semiconductor device of claim 12, wherein the insides of the first and second moats are filled with oxide.